of Okumura. All references are previously of record. Applicant submits the following arguments in traversal of the prior art rejections.

Applicant's invention relates to a two-dimensional type light modulation device. Detailed descriptions of the background and exemplary embodiment of the invention are set forth in the January 3, 2001 Amendment at pages 9-10 and in the October 5, 2001 Amendment at pages 4-5. Nakai is described in the January 3 Amendment at page 10 and Okumura is described in the October 5 Amendment at page 5. Applicant refers the Examiner to these descriptions.

The Examiner essentially repeats the rejections of the prior Office Action without rebuttal of many of the specific arguments previously of record. The Examiner offers only two general rebuttals with regard to the teachings of Nakai. These are addressed in turn.

First, the Examiner contends that "[c]ontrary to Applicant's arguments, the drive circuit taught by Nakai et al *is capable* of driving a circuit as claimed." (Emphasis added). Applicant would emphasize that the drive circuit of claims 2 and 8 writes data to the field effect transistors on the order of a row. Whether Nakai is capable of writing the data in this manner is not the correct assessment in determining anticipation. As set forth in the case In re Robertson, 49 USPQ2d 1949 (Fed. Cir. 1999), the teachings of the prior art do not support a prior art rejection if based on probabilities or possibilities. The Examiner is relying on such a presumed possibility that Nakai is capable of performing in the manner of the claimed drive circuit. Significantly, the Examiner has not provided any citation as to where such a capability is taught in the reference.

As a related matter, Applicant would argue that in the Robertson case, the Examiner attempted to rejected a claim reciting three fastening structures over a reference that taught only

two such structures. The Federal Circuit reversed the rejection of the U.S.P.T.O. stating that it was not proper to modify the existing structures of the references to have the capabilities of a missing claim feature. The present case is no different. In order to show writing data on a row order basis, Nakai must provide some indication that the drive circuit (e.g. 101, 104, 105 as cited by the Examiner) controls the operations of more than on pixel element in the matrix. There is no indication of this nature, and to impart such a feature would require reconfiguring the text or drawings, adding additional wiring connections, in a way not suggested by the reference. The anticipation rejection is not warranted.

Furthermore, it was previously argued that Nakai does not specifically describe matrix-wide control of the pixel electrodes, as the reference appears to suggest only control of one pixel electrode and associated drive circuitry. Applicant redirects the Examiner's attention to claim 6, for example, which describes selection of one electrode of a pixel exclusively.

Therefore, claims 2 and 8 are not anticipated for at least these reasons. Claims 3 and 9 which describe common driving of the pixels are also patentable in view of the individual control suggested by Nakai.

Second, with further regard to claims 4 and 12, the Examiner maintains that Nakai is certainly *capable* of changing a gate characteristic that effects a polarization change. Applicant argues there is no certainty about the Examiner's position, absent a reconfiguration of the reference. Applicant submits that Nakai uses the ferroelectric gate for a holding state. The Examiner's own citation at col. 4, lines 55-60 support this position. Applicant argues that Nakai does not change polarizations in the manner of the claims. Moreover, for the reasons set forth

above, the *capability* of Nakai is not the relevant inquiry, as it would rely on possibilities that cannot be relied upon in an anticipation rejection. The anticipation rejection of claims 4 and 12 should be withdrawn for this additional reason.

With further regard to claims 5, 11, 13, Applicant emphasizes that Nakai does not teach a ferroelectric gate transistor for row selection. To the extent the Examiner cites Okumura to make up for this deficiency, this would require a fundamental reconstruction of the Nakai reference, which is not warranted. Moreover, the single TFT transistor of Okumura does not comprise a single ferroelectric gate device as described by the claims.

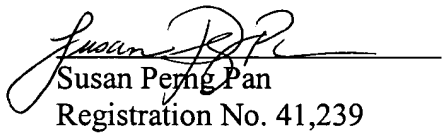
With further regard to claims 17-26, these claims describe a single ferroelectric gate transistor. Nakai clearly relies on the complementary structures of the dual conductivity type in order to effectuate its invention. Using only a single transistor would contradict this fundamental operation. See col. 5, lines 1-10. Modifications that contradict such basic principles of operation do not support obviousness rejections. Therefore, claims 17-26 are patentable for this additional reason.

Applicant would also redirect the Examiner to the arguments previously of record which remain pertinent and largely unrebutted in the record.

In view of the above, Applicant submits that claims 2-6 and 8-27 are in condition for allowance. Therefore it is respectfully requested that the subject application be passed to issue at the earliest possible time. The Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,



Susan Peng Pan
Registration No. 41,239

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: March 28, 2002